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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,302	07/06/2001	Rajiv V. Joshi	YOR9-2001-0512US1 (728-21	5687

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/900,302	Applicant(s) JOSHI ET AL.	
	Examiner James H. Cho	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-10* is/are rejected.

7)☒ Claim(s) *1,2,4,5 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 26, 2003 has been entered.

Claim Objections

2. Claims 1-2, 4-5 and 7-10 are objected to because of the following informalities:

"is output" on line 8 of claim 1 appears to be --is outputted--; "the said first" on line 2 of claim 2 appears to be --said first--; "first and second" on line 2 of claim 4 appears to be --said first and second--; "a third" on line 2 of claim 5 and on line 3 of claim 9 appears to be --the third-- respectively; "the output" on line 2 of claim 7 and on line 3 of claim 8 appears to be --, the output-- respectively; "of the three transistors" on line 2 of claim 8, and on line 3 of claim 9 should be deleted; "a first input" on line 4 of claim 10 appears to be --said first input--; and "output" on line 10 of claim 10 appears to be --outputted--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2 and 4-10 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sridhar et al. (US PAT No. 5,528,177). The response offers that for anticipation to be present each and every element of the claimed invention must be present in a single reference. The examiner agrees; hence:

<table>
<tr><th>Sridhar et al.

Fig. 2g (unless noted otherwise)</th><th>The claimed invention:</th></tr>
<tr><td>a logic circuit comprising 221, 222, 224</td><td>1. A MOSFET logic circuit for performing a logic OR operation comprising:</td></tr>
<tr><td>221, 222</td><td>a first and second transistors forming a transmission gate</td></tr>
<tr><td>a signal at the node 231</td><td>for outputting an intermediate signal,</td></tr>
<tr><td>A, B</td><td>where at least a first and second input signals are provided to the first and second transistors; and</td></tr>
<tr><td>224 provides an output signal at the node 231 by combining the output of 221 and 222 with a signal being pulled up by 224 (see table below)
<table><tr><th>A</th><th>B</th><th>/B</th><th>231</th></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr></table></td><td>a third transistor for providing an output to be combined with the intermediate signal to create an output signal indicative of an OR operation performed on the first and second input signals,</td></tr>
<tr><td>the signal at 231 is outputted to a CMOS inverter gate 232.</td><td>the output signal is output from the MOSFET logic circuit to any static CMOS logic gate.</td></tr>
</table>

222, 224	2. The MOSFET logic circuit as in claim 1, where the first and third transistors are PMOS transistors and
221	the second transistor is a NMOS transistor.
A is coupled to 221 and 222	4. The MOSFET logic circuit as in claim 1, where the first input signal is provided to a source of the first and second transistors,
B is coupled to the gate of 222	the second input signal is provided to a gate of the second transistor, and
/B is coupled to the gate of 221	a complement of the second input signal is provided to a gate of the first transistor.
/B is coupled to the gate of 224	5. The MOSFET logic circuit as in claim 1 where a complement of the second input is provided to a gate of the third transistor.
/B is coupled to the gate of 224	6. The MOSFET logic circuit as in claim 1 further providing a third input signal to the third transistor, the third input signal being a complement of the second input signal.
B is a logic low, the output at 231 is the output of 221 and 222 since 224 is being turned off by /B	7. The MOSFET logic circuit as in claim 1 where when the second input signal has a logic LOW level, the output of the MOSFET logic circuit is an output signal of the transmission gate.

224 pulls the signal at 321 up to a logic high when its gate voltage /B is logic low, i.e. the second input signal B is a logic high.	8. The MOSFET logic circuit as in claim 1 where the third transistor is a pull-up transistor, and when the second input signal has a logic high level, the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic high.
delay through 221 and 222 and turn-on delay of 224	9. The MOSFET logic circuit as in claim 1, where a delay of the MOSFET logic circuit is one of a delay of the transmission gate formed by first and second transistors and a delay of the third transistor.
a logic circuit comprising 221, 222, 224	10. A logic OR circuit comprising:
a transmission gate comprising nMOS 221 receiving A, and pMOS 222 receiving A and B at the gate	a transmission gate for outputting a first intermediate output signal, the transmission gate being formed by a pMOS transistor receiving a first input signal and a nMOS transistor receiving said first input signal, where a gate of the pMOS transistor receives a second input signal; and
pMOS 224 receives /B	a pull-up pMOS transistor receiving a complement of the second input signal,

<table>
<tr>
<td>224 provides an output signal at the node 231 by combining the output of 221 and 222 with a signal being pulled up by 224 (see table below)
<table><tr><th>A</th><th>B</th><th>/B</th><th>231</th></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr></table></td>
<td>the pull-up pMOS transistor providing a second intermediate output signal for combining with the first intermediate output signal to create an OR output signal, where the OR output signal is indicative of an OR operation performed on the first and second input signals,</td>
</tr>
<tr>
<td>the signal at 231 is outputted to a CMOS inverter gate 232.</td>
<td>the OR output signal is outputted from the OR logic circuit to any static CMOS logic gate.</td>
</tr>
</table>

Response to Remarks

4. Applicant's remarks filed June 26, 2003 have been fully considered but they are not deemed to be persuasive regarding claims 1-2 and 4-9.

On page 4 of the amendment, applicant argues that "The Sridhar circuit in Fig. 2g requires the inverter 232 to provide the same OR output..." and "The output of the inventive three-transistor circuit without the use of the inverter".

However, the examiner notes that the logic circuit comprising 221, 222, and 224 in Fig. 2g having an output node 231 meets all limitation of the claimed invention, which performs a logic OR operation as discussed in the rejection of claims. The output at the output node 231 does not require an inverter to perform the logic OR operation where the inverter is added to perform a NOR operation.

Applicant further argues that Sridhar does not teaches or describes "providing an output to be combined with said intermediate signal to create an output signal indicative

of an OR operation performed on said first and second input signals, said output signal is output from the MOSFET logic circuit to any static CMOS logic gate".

However, the examiner notes that the output signal at the output node 231 is a combination of "an intermediate signal", i.e. the output of the transmission gate comprising 221 and 222 and the output of 224 where the 224 performs a pull-up function when enabled by its gate signal, /B and 221 and 222, performs a transmission gate function defined by the signal A, B, /B and the OR output is outputted to an input of a CMOS logic gate inverter 232 to give a NOR output.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

James H. Cho
Examiner
Art Unit 2819

July 11, 2003